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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

YE, LIN

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 04/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/337,494

Applicant(s)

MATOBA ET AL.

Examiner

Lin Ye

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 and 29-40 is/are rejected.
- 7) ☒ Claim(s) 26-28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-40 filed on 3/8/04 have been considered but are moot in view of the new ground(s) of rejection. This action is non-final.
2. Applicant states "claims 32-41 have been added" on the remarks/arguments on page 14, lines 3. However, It should be noted that there has no claim 41 disclosed in the amendment filed on 3/08/04.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
4. Claims 1-4, 12-14, 18-20, 22-23, 24-25, 30-33 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama U.S. Patent 6,512,791 in view of Miyake et al. U.S. Publication 2002/0102027.

Referring to claim 1, the Takayama reference discloses in Figures 6A-D and 9-10, an image processing unit comprising: an A/D converter (16) for carrying out A/D conversion of image signals output from an image pickup apparatus (CCD 12) that picks up an image and converts it into electrical signals, and for outputting A/D converted image singles as image

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data as shown in Figure 10; a coding circuit (the orthogonal transformer 104, the quantizer 106 and the coder 107) for dividing the image data into unit blocks, each comprising a predetermined number of pixels (predetermined to be 8x8 pixels, See Col. 5, lines 63-67) as shown in Figure 6C, and for coding the pixels in each unit block after obtaining an average level (the average brightness level of 8x8 pixels is obtained) of the pixels in the unit block (See Col. 6, lines 1-5); an exposure controller (system controller 100) for calculating a luminance level of a whole set of pixel data in the unit blocks by integrating the average levels of the unit blocks, and for controlling exposure of the image pickup apparatus such that the luminance level of the image data matches a predetermined level (See Col. 9, lines 35-40). However, the Takayama reference does not explicitly show the coding circuit also including a fixed-length coding method that can output the image data having a fixed length.

The Miyake reference discloses in Figure 46, an image-processing unit comprising a compression processor (2235). The compression processor including a block circuit (2041) for dividing the image data into unit blocks, each comprising a predetermined number of pixels (8x8), a discrete cosine transforms circuit (DCT 2043) and a fixed length coding circuit (fixed-length encoder 2002) for coding the pixels in each unit block, wherein a length of the code output from the fixed length coding circuit is fixed on a block-by-block (See page 23 [0459], page 24, [0471], [0482] and page 14 [0291]). The Miyake reference is an evidence that one of ordinary skill in the art at the time to see more advantages for an image-processing unit has more flexible options to select either a fixed-length coding method or variable-length coding method for compressing image data instead only variable-length coding alone, so that if a code amount becomes larger than expected in variable-length

coding, the fixed-length coding method is very effective as a final means. For that reason, it would have been obvious to see the image-processing unit comprising a fixed length coding circuit output the image data having a fixed length disclosed by Takayama.

Referring to claim 2, the Takayama and Miyake references disclose all subject matter as discussed in respected claim 1, and Miyake reference also disclose coded image memory (2036) for storing fixed length coded data output from the fixed length coding circuit, the fixed length coded data including the average levels of the unit blocks (See Figures 2 and 46, Page 4 [0102]).

Referring to claim 3, the Takayama reference discloses the system controller (100) decoding for the fixed length coded data with performing gain correction for adjusting the luminance level of the image data to a predetermined level (See Col. 6, lines 36-44).

Referring to claim 4, the Miyake reference discloses a fixed length decoding circuit (expansion processor 19 as shown in Figure 1, see Page 4 [0098]) for reading from said coded image memory the fixed length coded data, and for carrying out fixed length decoding of the fixed length coded data; and a signal processor (orthogonal inverse transform circuit) for carrying out, using the average levels, gain correction (the Takayama reference already discloses the fixed length coding data contents the information about the average levels, gain correction) of image data output from said fixed length decoding circuit (See Col. 7, lines 53-66).

Referring to claims 12-14, the Takayama reference discloses comprising selecting means for selecting a number and location of unit blocks as shown in Figure 6D-6E (selecting the blocks in the central area of screen in Figure 6D, and the area which was designated by

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manual selection in Figure 6E, See Col. 6, lines 59-63); for selecting the unit blocks (8x8 pixels) in accordance with their average levels (See Col. 6, lines 1-5).

For claim 18, the Takayama reference discloses all subject matter as discussed with respected to same comment as with claim 1.

For claims 19-20 and 22-23, the Takayama reference discloses all subject matter as discussed with respected to same comment as with claim 1.

For claims 24-25 and 30, the Takayama reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 31, the Takayama reference discloses the system controller (100) calculating a gain correction coefficient needed to correct the luminance level of the digital image data to a predetermined luminance level; and adjusting the luminance level of the digital image data based on the gain correction coefficient (See Col. 6, lines 36-44).

Referring to claim 32, the Miyake reference disclosed wherein the length of the code output from the fixed length coding circuit is fixed for each unit block (See Page 14 [0291]).

For claim 33, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 4.

For claim 36, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 32.

For claim 37, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 33.

For claim 38, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 32.

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For claim 39, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 33.

For claim 40, the Takayama and Miyake references disclose all subject matter as discussed with respected to same comment as with claim 4.

5. Claims 5-11, 15-17, 21, 29 and 34-35, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama U.S. Patent 6,512,791 in view of Miyake et al. U.S. Publication 2002/0102027 and Iwasaki et al. U.S. Patent 5,414,487.

Referring to claims 5 and 7, the Takayama and Miyake references disclose all subject matter as discussed in respected claim 1, except the reference does not explicitly show a pixel rearrangement circuit for sorting the image data that each color component is arranged in a unit block, and the image unit has signal level correction means respective color components.

The Iwasaki reference discloses in Figures 17 and 19A-B, an AE camera including a pixel rearrangement circuit (grouping device 49) for grouping the image data in a checkerboard pattern which each color component is arranged in a same group (unit block), each of which consists of a predetermined number of pixels (3x3 pixels) (See Col. 12, lines 35-39). The Iwasaki reference is evidence that one of ordinary skill in the art at the time to see more advantages for an image-processing unit including a pixel rearrangement circuit to group each color component in a unit block so that a shift in light metering portion due to a color difference can be further reduced. For that reason, it would have been obvious to see the image-processing unit comprising a pixel rearrangement circuit for sorting the image data that each color component is arranged in a unit block and the signal level correction means respective color components disclosed by Takayama.

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For claim 6, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claims 1 and 5.

For claim 8, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claim 2.

For claim 9, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claims 2 and 7.

For claim 10-11, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claims 4 and 7.

For claim 15-17, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claims 5 and 12-14.

For claim 21, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claim 5.

For claim 29, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claim 5.

For claim 34, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claim 32.

For claim 35, the Takayama, Miyake and Iwasaki references disclose all subject matter as discussed with respected to same comment as with claim 33.

Allowable Subject Matter

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6. Claims 26-28 are objected to as being dependent upon a rejected base claim 24, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Schwartz U.S. Patent 2003/0138151 defined fixed-length coding which is a system that converts a specific block of data to a specific block of compressed data.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive,
Arlington, VA., Sixth Floor (Receptionist).

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Lin Ye
March 30, 2004



NGOC-YEN VU
PRIMARY EXAMINER